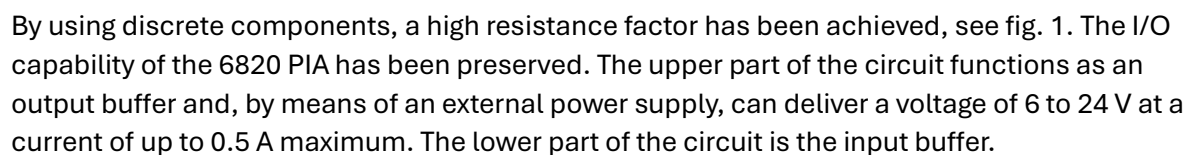




The outputs of the user PIA are not suitable for connecting devices to. A buffer stage is necessary to achieve this. I believe that the term "student-proof" applies to this circuit.



The A-side of the PIA has an output stage consisting of a FET with a resistor in the drain lead. If the circuit of fig. 1 is connected to this, R1 is not needed; T2 can simply be placed in parallel with the FET.

The B-side of the PIA has a tristate output. This is a "totem pole" in which both transistors can be cut off (see Applications Manual pages 3 through 11). For this, a genuine signal voltage must be fed in. Therefore, resistor R1 is indeed necessary for the B-side. The PIA has a total of twenty output points for signals, of which two are exclusively inputs (CA1 and CB1). The remaining eighteen are bi-directional. This means that the upper part of the circuit must be present eighteen times and the lower part twice. The whole thing easily fits on a board the same size as the CPU board. Both boards can then be mounted in parallel inside a housing.

No special requirements apply to transistors T1, T2 and T3. T4 is a somewhat more robust PNP,

for example a 2N2905. No special requirements apply to diodes D1, D2, D3 and D4 either. D5 is a somewhat larger silicon type of about 5 A.

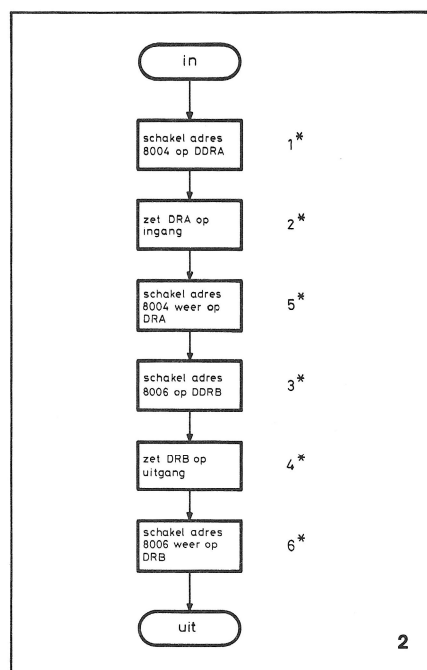
This diode serves to prevent problems with the μP supply if something goes wrong with the external power supply.

D4 serves to protect T4 against voltage spikes that can occur with inductive loads such as relays and small motors.

LEDs can be connected to the output terminals. When tinkering with programs, this allows the output signals to be observed quickly. Should the current load caused by this become a problem at some point, it is convenient to be able to switch off the LEDs with S1.

You can safely leave out capacitor C1. The maximum switching frequency at the input is then around 20 kHz. That is more than sufficient for the simplest applications. Placing C1 in the input circuit of T1 significantly increases the maximum achievable frequency. For optimal effect, it is best to determine the value of C1 experimentally.

The output is intended for a current-sinking load, such as small lamps, relays, etc. The output impedance of the stage is approximately $0\ \Omega$ due to the conducting state of T4. For current-sourcing loads, the output resistance is $2.2\ \text{k}\Omega$, which is the cut-off state of T4. In that case, no significant current load is possible. Reducing the collector resistance is of course undesirable. The only good solution would be a totem-pole output, but that would make the circuit rather complicated. Current-sourcing loads occur only rarely, however; in that occasional case, it is better to provide the load with an inverting stage.



PIA initialization

The initialization listed in table 3 for the user PIA sets all data lines of the A port to input and all data lines of the B port to output. The flowchart is shown in fig. 2. Tables 1 and 2 show the abbreviations and indicate at which address what must happen in order to select which register is addressed. Once these lines are buffered, it is best to start with a number of very simple exercises. To do this, connect a small lamp to an output line (you can choose the voltage yourself!) and connect a pushbutton to an input line (make contact to 0 V).

Table 1

DRA is Data Register A
 DDRA is Data Direction Register A
 CRA is Control Register A
 DRB is Data Register B
 DDRB is Data Direction Register B
 CRB is Control Register B

Table 2

Adres	CRA-bit 2 = „1"		CRA-bit 2 = „0"
8004	DRA	or	DDRA
8005	CRA		
Adres	CRB-bit 2 = „1"		CRB-bit 2 = „0"
8006	DRB	or	DDRB
8007	CRB		

Table 3

	Address	Opcode	Objectcode	Mnemonics
start	00 20	86	00	LDA A #
1		B7	80 05	STA .
2		B7	80 04	STA A
3		B7	80 07	
		86	FF	LDA #
4		B7	80 06	STA .
		86	04	LDA #
5		B7	80 05	STA
6	00 34	B7	80 07	